A Dual Bus Approach for LAN Interworking With ATM Networks[1]

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ABSTRACT

The interworking between conventional legacy LANs and the ATM network plays an important role in the initial step of the ATM roadmap. This paper presents a dual bus approach for connecting LAN interworking units (IWU) *to ATM networks. Several IWUs connecting heterogeneous LANs are configured into a dual bus structure and the end of the buses are directly connected to the ATM ports. Each IWU transforms the connectionless frame from the legacy LAN to fixed-length time-slots on the dual bus. To provide reliable connectionless services, a cell-based flow control scheme is proposed for dynamically adjusting the cell input rate so as to match with the current resources in the ATM switch. The scheme is further verified to be able to provide an optimal, best-effort and reliable interconnection scenario through simulations. The results show that the total throughput obtained by each local subnetwork dynamically matches with the cell processing throughput of the ATM switch. Besides, each IWU on the dual bus shares a fair bandwidth.*

1 Introduction

ATM (Asynchronous Transfer Mode) is the standard recommended by ITU-T (International Telecommunication Union, Telecommunication Standardization Sector) and ATM Forum for implementing the broadband ISDN [1], [2]. ATM local area networks and long distance ATM trial are currently being built by the research groups all over the world [3], [4]. For users on a traditional LAN to benefit from ATM, it is essential to provide the interworking capability between them. Recently, two emerging standards for interworking between IEEE 802.X LANs and ATM networks are defined, namely the *LAN emulation* adopted by ATM Forum and the *IP over ATM* proposed by IETF (Internet Engineering Task force) [5], [6]. Both schemes use an *Interworking Unit (IWU)* to perform the required interworking functions such as connectivity, protocol conversion, address mapping, and congestion control.

It is often necessary for an ATM switch to interwork with more than one legacy LANs of hetergeneous types, i.e., Ethernet, Token ring, FDDI, and Fast Ethernet. There are three methods to interconnect these

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IWUs to the ATM switch. The first method is called the *one-to-one dedicate* approach which elaborates one IWU for each LAN and each IWU is connected to an ATM port, as shown in Figure 1a. This approach is not efficient because of the low utilization in each ATM port. Another method is called the *concentrated* approach which elaborates one IWU for all the legacy LANs, as shown in Figure 1b. This approach has high utilization as the number of ATM ports are saved. However, it requires a set of centralized control functions all embedded in one IWU, i.e., flow/congestion control, priority control, packet format transformation, segmentation/reassembly, ..., etc. The above mechanism is even more complicated when the aggregate throughput of all the legacy LANs is higher than the maximum throughput of a single ATM port. The third method we proposed is called the *distributed dual bus (DDB)* approach which elaborates one IWU for each LAN and these IWUs are interconnected by a high-speed, distributed dual bus, as shown in Figure 1c. This approach is simple and efficient for interworking with multiple legacy LANs to ATM because of the following reasons:

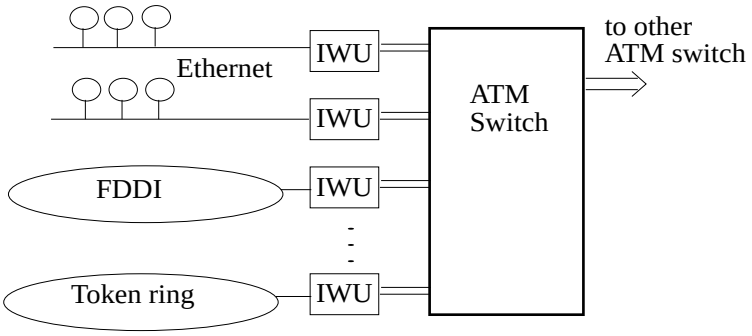
- The interworking function for each LAN is executed seperately and independently.
- The function for LAN access to ATM is performed distributedly over the dual bus.

The DDB method is briefly described as follows. Each IWU performs the protocol conversion between the legacy LAN MAC and the ATM layer. The data flow on the dual bus is structured into fixed-length time-slots which are intended for carrying the ATM cells. Therefore, the speed of the bus should be equal to the speed of the ATM port, i.e., typically 155 Mbps. The operation of the DDB method requires a distributed control protocol for each IWU to access the time-slots. Various access methods can be adopted on the dual bus such as, *IEEE 802.6 Distributed Queue Dual Bus (DQDB)*, the *Fair Distributed Queue (FDQ)*, and the *Slot Interleaved Multiple Access (SIMA)* [7], [8], [9]. In this paper, we select DQDB as the access method for describing the proposed scheme. To carry the ATM cells on the dual bus, the ATM cell format is encapsulated by two additional octets, namely the *Access Control Field (ACF)* and the *Flow Control Field (FCF)*, as shown in Figure 2. The ACF octet is used by the dual bus access protocol for access the empty slot. To operate the system efficiently, a flow control mechanism is essential. The FCF octet is reserved for the flow control which will be proposed and described later. The flow control is activated distributedly in between each IWU and the ATM switch to guarantee a reliable transmission. This paper will focus on the flow control method which cooperates within the DDB approach and makes a more efficient and reliable system.

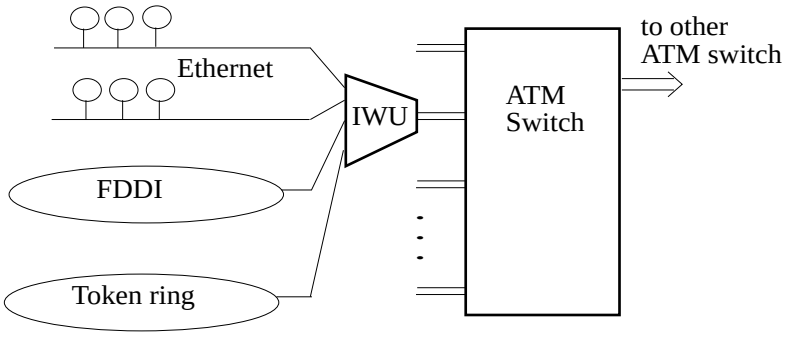
The organization of this paper is as follows. In section 2, the system architecture of the DDB method is briefly describbed. In section 3, the cell-based flow control scheme is described and an example is given. In section 4, some definitions for performance measurement and simulation model are defined. The simulation results are demonstrated in section 5. A short conclusion is made in section 6.

2 System Architecture

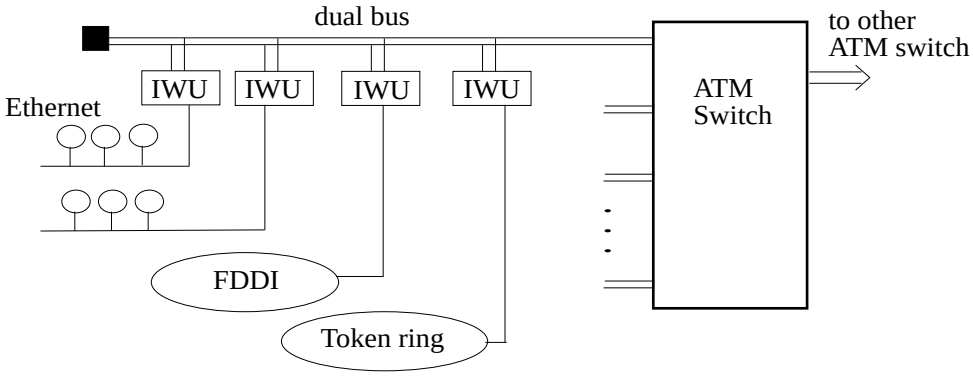
For simplicity, the dual bus structure connecting multiple IWUs is referred to as the DQDB subnetwork throughout this paper. The DDB system architecture is shown in Figure 3. In this configuration, the IWUs are connected to the DQDB subnetwork via *bus A* (the forward bus) and *bus B* (the reverse bus). An ATM switch with finite input buffer is capable of providing the cell-switching capabilities between



(a). The one-to-one dedicate approach.



(b). The concentrated approach.



(c). The distributed dual bus approach.

Figure 1: The interworking between multiple legacy LANs and ATM.

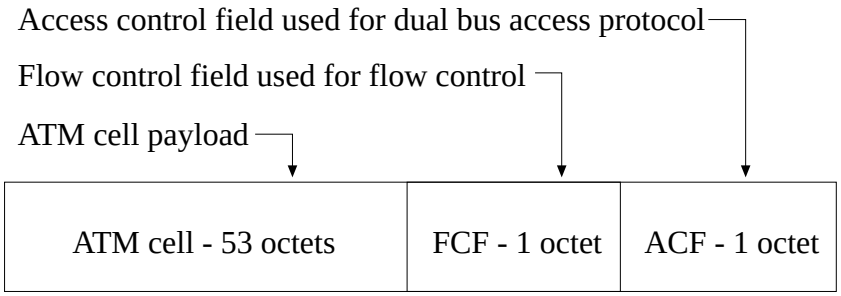


Figure 2: The slot format on the dual bus.

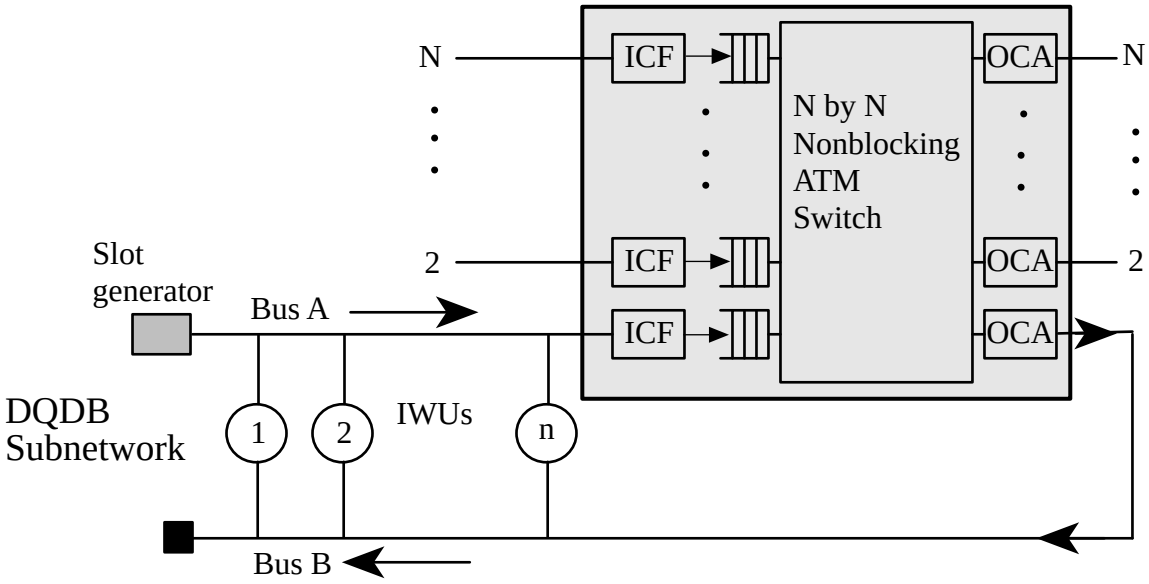


Figure 3: The DDB system architecture.

the *N* input lines and the *N* output lines. The end of bus A is connected to one of the input lines for feeding DQDB slots to the ATM switch. The head of bus B is connected to one of the output lines for receiving cells from the ATM switch.

The local traffic between two IWUs can also be carried by the dual bus. Since all kinds of the frame formats are converted into cells, the communication between two heterogeneous LANs is also very simple. This traffic is referred to as the local traffic. The traffic which transmitting cells to the ATM switch is called the remote traffic. Two additional mechanisms are required for the remote traffic. An *Input Cell Filter (ICF)* is placed between the end of bus A and the ATM input buffer for filtering cells, as shown in Figure 3. Each *ICF* has a filtering database for distinguishing local cells from remote cells. An *Output Cell Arbitrator (OCA)* is placed between the head of bus B and the output line of the ATM switch for controlling the ratio of remote traffic to local traffic on bus B. For remote traffic, the *OCA* activates the corresponding output line, receives a cell from the switch and injects the cell into bus B. For local traffic, the *OCA* deactivates the corresponding output line and generates an empty slot into bus B. In this system, if an output line is inactive, then no cell is allowed to be switched from any one of the

input lines to this output line.

The ATM switch is assumed to be a nonblocking switch with finite input capacity. By nonblocking we mean that any two cells will not be blocked internally if they are destined to different output lines. If there are multiple cells destined to the same output line, only one of them can be switched and the others must be queued. Since the input buffer is limited, a remote cell coming from bus A may be dropped if there is no available buffer for it. To provide a reliable communication for the proposed interconnection system, an efficient flow control scheme is necessary. Two flow control methods are commonly used for current computer communications, the *window-based* method and the *rate-based* method. In the window-based method, the user is permitted to transmit up to a fixed amount of data (the window size) whenever a confirmation is received [10], [11]. Then, the user stops and waits until another confirmation is received. A larger window size can produce a higher throughput but also results in a higher packet loss rate. On the contrary, a smaller window size can produce a lower packet loss rate but results in a lower throughput. The other method called rate-based flow control is proposed due to the high-speed requirement of the ATM (Asynchronous Transfer Mode) networks [12]. Since the size of each ATM cell is small and fixed, it is more efficient to regulate the cell transmission rate rather than to control the transmission volume. But the rate-based scheme requires some additional mechanisms such as the traffic monitoring, leaky bucket, rate control and adjuctment, ..., etc.

We propose a simple flow control mechanism called *Cell-Based Flow Control* for the DDB method. In this scheme, the remote traffic is transmitted into the ATM switch in a cell-by-cell request-confirm fashion. An IWU on bus A of the DQDB subnetwork is permitted to transmit a remote cell destined to the ATM switch if and only if it receives a confirmation on bus B from the ATM switch. The network congestion is effectively prevented by the proposed scheme since no segment is lost in the ATM switch, and in the meantime, the transmission throughput of the interconnection system is maximized.

The performance of the proposed scheme is evaluated by simulations. The results show that the total throughput obtained by each DQDB subnetwork dynamically matches with the cell processing throughput of the ATM switch. Besides, each station on the DQDB subnetwork shares a fair bandwidth. In the next section, the cell-based flow control scheme is described in detail.

3 A Cell-Based Flow Control Scheme

The key feature of the DQDB protocol is described before the proposed scheme is introduced. The DQDB Media Access Control (MAC) protocol is a standard defined by the IEEE 802.6 for local and metropolitan area networks. Two modes of MAC access are provided: non-arbitrated (NA) access and queued-arbitrated (QA) access. For connectionless service, we consider only the QA access method. The basic QA access method is described as follows. At the head of bus A, fixed-length slots are generated periodically from upstream to downstream (in this paper, stations near the head of bus A are referred to as the upstream stations). Each slot consists of 53 bytes in which the first byte is the *Access Control Field (ACF)* containing a BUSY bit and a three-bit REQUEST field. The BUSY bit is used to indicate whether or not a slot is used. Each of the three REQUEST bits is used to inform the upstream stations that an additional QA segment with a particular priority level had occupied a position in the distributed queue. Each station maintains two counters for each of the three priority level: the Request Counter (RC) and the CountDown Counter (CD). The Distributed Queuing Machine has two states called IDLE state and

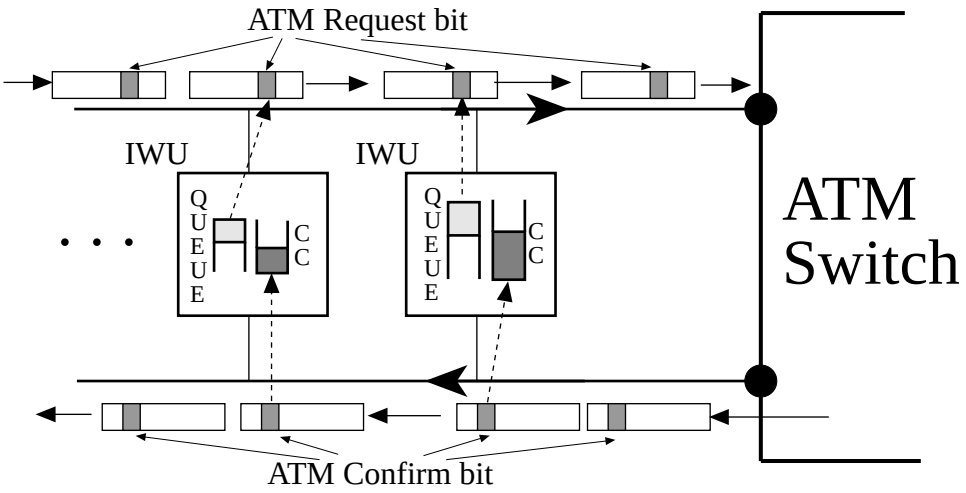


Figure 4: A paradigm of the cell-based flow control.

COUNTDOWN state. In each IDLE station, the value of RC is incremented by 1 for each non_zero request going upstream on bus B, and is decremented by 1 for each empty slot going downstream on bus A. When a station is to access the bus A, it sends a request to all upstream stations by allocating a zero REQUEST bit on bus B, downloads the value of RC to CD, resets the value of RC, and transits itself to COUNTDOWN state. In this state, a station also increments the value of RC by 1 for each non_zero request going upstream on bus B but decreases the value of CD by 1 for each empty slot going downstream on bus A. When the value of CD goes to zero, the station is allowed to access the next empty slot on bus A. After the station had accessed the slot, it enters the IDLE state again.

In Figure 3, the input buffer of the ATM switch is located at the end of bus A of the DQDB subnetwork. Under heavy load, there is a cell arrival in almost every slot time. If the cell processing rate in the ATM switch is not fast enough, the cell loss rate is very high. Thus, the cell transmission from the DQDB subnetwork to the ATM input buffer should be in an on-demand fashion. Two additional bits in the FCF octet of the slot header are used to achieve this goal: the ATM_REQUEST bit and the ATM_CONFIRM bit. The ATM_REQUEST bit is used by the stations on bus A for requesting a space in the ATM input buffer for each new segment queued for transmission. The ATM_CONFIRM bit is sent on bus B by the ATM input buffer controllor to confirm that a space for another new cell is ready. A paradigm of this operation is shown in Figure 4. The non-zero ATM_REQUEST bit represents that a remote segment in the upstream has already entered the distributed queue and is waiting for a confirmation from the input buffer. The zero ATM_CONFIRM bit represents a confirmation sent by the ATM switch and indicates that there is a space in the input buffer for holding another one segment (cell). Each active station maintains a *credit counter (CC)* for collecting the confirmations from the ATM switch. The ATM_CONFIRM bit should not be reused, since one confirmation can match with only one queued segment. Thus, after a station receives a confirmation (the zero ATM_CONFIRM bit), the value of the ATM_CONFIRM bit should be changed into 1. When there is no active station waiting for confirmations, the ATM switch always sends non-zero ATM_CONFIRM bits into bus B.

Using the above mechanism, three algorithms should be further designed for the proposed scheme to

achieve a better performance of the system, as listed below.

- In the ATM switch, a *credit generating algorithm* is necessary in order to confirm the requests from bus A.
- The credits generated by the ATM switch should be fairly shared by all the active stations on bus B of the DQDB subnetwork. Thus, a fair *credit distribution protocol* is necessary for the DQDB subnetwork.
- To avoid the system to behave like a stop-and-wait system, the *multiple requests outstanding* strategy should be used to increase the throughput.

The details of the above three algorithms are presented in the following subsections.

3.1 The Credit Generating Algorithm

Two counters are maintained in the ATM switch for the credit generation. The *ATM Request counter (ARQ)* is used to count the number of non-zero ATM_REQUEST bits from bus A. The *Confirmed Space counter (CS)* is used to reserve the space for the credits sent by the ATM switch. Assume that the total capacity of the ATM input buffer is b and the current number of cells queued in the input buffer is q (in unit of cells), the procedures of the credit generating algorithm are described as follows.

Algorithm CG (Credit Generating)

The following procedures are executed in every slot time:

1. *ARQ = ARQ + 1* for each incoming non-zero ATM_REQUEST bit on bus A.
2. $CS = CS - 1$ and $q = q + 1$ for each incoming remote segment from the *ICF*.
3. If $ARQ > 0$ and $CS + q < b$, then a zero ATM_CONFIRM bit is sent on bus B, *CS = CS + 1* and *ARQ = ARQ - 1*.

The relation between the above counters and the parameters is shown in Figure 5. Certainly, the value of q will be decremented by 1 if a queued cell in the input buffer is routed to one of the output lines. The counter CS is incremented by 1 for each credit sent and is decremented by 1 for each new incoming cell. Thus, the value of CS represents the expected number of cells that will arrive in the near future. That is, the value $CS + q$ represents the expected queue length of the input buffer in the near future.

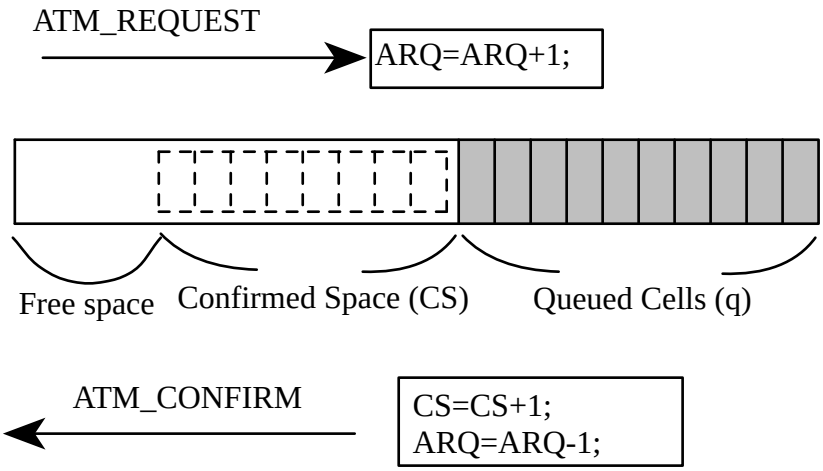


Figure 5: The parameters for credit generation in the ATM input buffer.

3.2 The Credit Distribution Protocol

To fairly share the credits on bus B, the Distributed Queuing Machine defined by the IEEE 802.6 standard is not considered to be usable because:

1. The Distributed Queuing Machine is not fair without the Bandwidth Balancing Mechanism (BBM) [7].

2. With the BBM, the credit may be lost. This may cause a station to keep waiting for a credit from the ATM switch, but the ATM switch has sent the credit out and keep waiting for a new arriving cell (deadlock condition).

Recently, many fair distributed queuing methods were proposed to overcome the drawbacks of the original DQDB standard [13], [8]. For our flow control, the scheme called *Slot Interleaved Multiple Access (SIMA)* which we have proposed in [9] is used. In this scheme, each station transits itself into the *active* state if it has segments queued for transmission. Each station keeps the number of downstream active stations (excluding itself) by an *active counter* AC. A countdown counter CD is used to bypass empty slots to the downstream. Initially, the value of CD equals to AC. The value of CD is decremented by 1 for each empty slot going downstream. When the value of CD goes to zero, the station is allowed to access the next empty slot, and then, downloads the value of AC to CD, and begins to count down again. In another words, a number of AC empty slots will be bypassed unconditionally after a station has transmitted a segment.

We use the SIMA scheme on bus B to fairly share the credits. In this case, we still refer to the upstream (downstream) stations as the stations near the head of bus A (near the ATM switch). Two additional bits in the FCF octet, the ATM_START bit and the ATM_END bit are used to inform the downstream stations that an upstream station has just changed into active state or inactive state. Two counters ATM_AC and ATM_CD are maintained in each station. The ATM_AC is used to keep the number of upstream active stations, i.e., increases (decreases) by 1 for each non_zero ATM_START (ATM_END) bit received on bus A. The ATM_CD is used to bypass ATM_AC zero credits to the upstream stations.

On bus A, we need another distributed queuing protocol to fairly share the empty slots. Either the original DQDB standard or the SIMA scheme can be employed. Each time a station wants to transmit a remote segment, it begins to send a request to the ATM switch by a zero ATM_REQUEST bit on bus A. In the mean time, it begins to count the empty slots on bus A via the countdown counter CD (note that both DQDB standard and the SIMA scheme have a countdown counter CD). The station can not transmit a remote segment on an empty slot of bus A until the counter CD is zero and a credit from the ATM switch is received. Thus, the new condition for a station can transmit a remote segment is : *CD = 0 and a zero ATM_CONFIRM is received*.

3.3 Multiple Requests Outstanding

If each station can request only one ATM credit before it can transmit the next remote segment, the system will perform like a stop-and-wait system. To achieve a higher throughput, the *Multiple Requests Outstanding (MRO)* mechanism can be used. When a station is waiting for a confirmation and there are still many segments awaiting in the local queue, another remote request can be put into a zero ATM_REQUEST bit before the credit arrives. Two additional counters, the *Outstanding Request Counter (ORC)* and the *Confirm Counter (CC)* are maintained in each station. The following algorithm is executed in each station to perform the *MRO* mechanism.

Algorithm MRO (Multiple Requests Outstanding)

The following procedures are executed in every slot time:

1. If there are arrivals of k new remote segments from the users, then $ORC = ORC + k$;
2. If $ORC > 0$ and a zero ATM_REQUEST bit arrives, then $ORC = ORC - 1$ and write "1" into the ATM_REQUEST bit;
3. If a station receives a zero ATM_CONFIRM, then $CC = CC + 1$ and write "1" into the ATM_CONFIRM bit;
4. If a station successfully transmits a remote segment, then $CC = CC - 1$;
5. A station can transmit a remote segment if and only if *CD = 0 and CC* > 0.

3.4 A Summary of the Scheme and An Example

To use the cell-based flow control scheme, there are four additional control bits required in the cell header, the ATM_REQUEST bit, the ATM_CONFIRM bit, the ATM_START bit and the ATM_END bit. In each station, four additional counters should be maintained, the *ATM_AC* counter, the *ATM_CD* counter, the *CC* counter and the *ORC* counter. An example of the cell-based flow control scheme on the DQDB subnetwork with three stations is given in Figure 6(a) throughout Figure 6(f). Figure 6(a) shows

the control bits and counters required in this example. In Figure 6(b), station 3 becomes active. It sends a non_zero ATM_REQUEST on bus A and sends a non_zero REQUEST on bus B. In Figure 6(c), station 1 becomes active. It sends a non_zero ATM_REQUEST on bus A and sends a non_zero REQUEST on bus B. Also, station 3 gets a zero ATM_CONFIRM from bus B. In Figure 6(d), station 2 becomes active. It sends a non_zero ATM_REQUEST on bus A and sends a non_zero REQUEST on bus B. Also, station 1 gets a zero ATM_CONFIRM from bus B and station 3 gets an access to an empty slot on bus A. In Figure 6(e), station 2 gets a zero ATM_CONFIRM from bus B and station 1 gets an access to an empty slot on bus A. In Figure 6(f), station 1 gets an access to an empty slot on bus A.

The deadlock condition mentioned in subsection 2.2 may still occur when we use the *SIMA* protocol instead of the *BWB* mechanism. However, the probability is reduced. To avoid the deadlock condition, we assume that the head of bus A would send a busy slot to flush the confirmed space of the input buffer when a zero ATM_CONFIRM bit is collected at the end of bus B.

The *OCA (Output Cell Arbitrator)* on each output line of the ATM switch is for controlling the ratio of the remote segments to the local segments in each of the DQDB subnetworks. For simplicity, the ratio is denoted as *R/L*, where R and L are integers. Within every $(R + L)$ slot times, the *OCA* should transmit at least L empty slots to bus B and the rest slot times are reserved for transmitting remote segments.

4 Performance Measurement and the Simulation Model

4.1 Performance Measurement

The performance of the cell-based flow control scheme is evaluated in terms of the following metrics:

ATM Switching Throughput (AST) = the average number of segments received by the ATM input buffer per slot time.

ATM Cell Loss Rate (ACLR) = the average number of segments lost in the ATM input buffer per slot time.

DQDB Station Throughput (DST) = the average number of segments transmitted by a DQDB station per slot time.

Assume that the number of stations on the DQDB subnetwork is n and let DST_i denote the throughput of the i-th station on the DQDB, $1 \leq i \leq n$. Then, the **Total DQDB Throughput (TDT)** is defined by

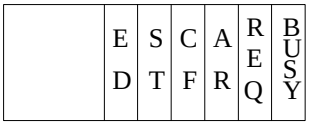
$$TDT = \sum_{i=1}^{n} DST_i$$

The performance of the ATM switch is measured by AST and $ACLR$. A high performance system would require a high AST and a low $ACLR$. To evaluate the performance by one metric, we define the **ATM Switching Efficiency (ASE)** by

$$ASE = \frac{AST}{1 + ACLR \times LOSS\_PENALTY}$$

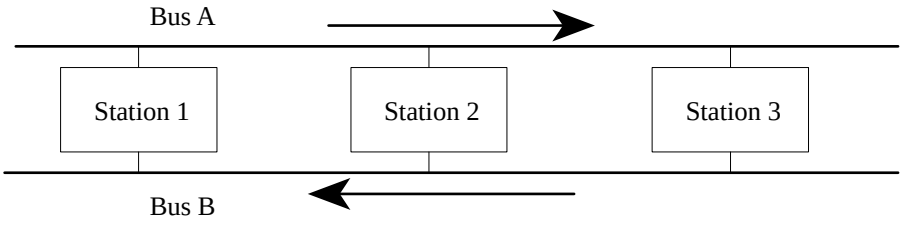
where the *LOSS_PENALTY* is a constant which represents the penalty due to data retransmissions when there are cells lost in the ATM switch. The constant 1 in the divider is to avoid the divide-by-zero effect

(6a)

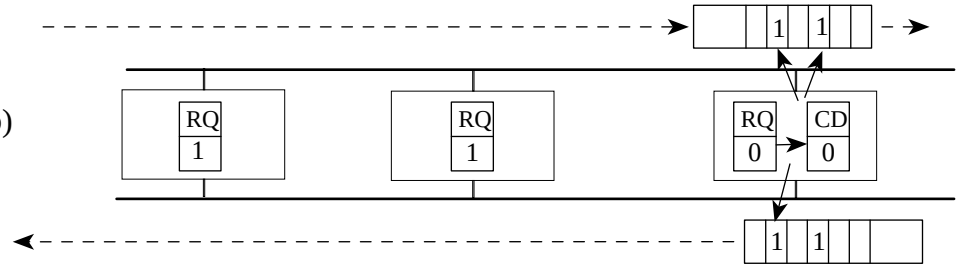


Control bits:
AR: ATM_REQUEST,
CF: ATM_CONFIRM,
ST: ATM_START,
ED: ATM_END.

Counters:
AA: ATM Active Counter,
CC: ATM Confirm Counter,
RQ: Request Counter,
CD: CountDown Counter.



(6b)



(6c)

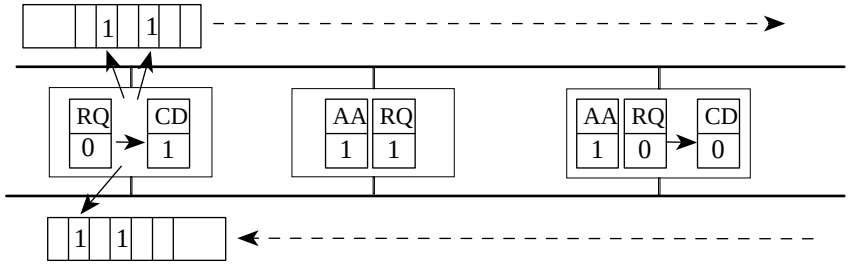
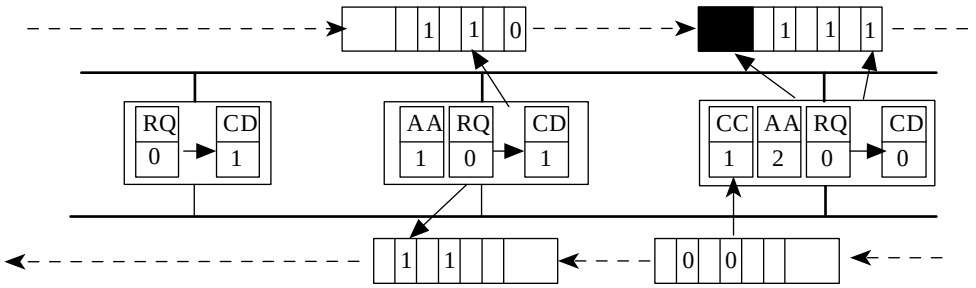
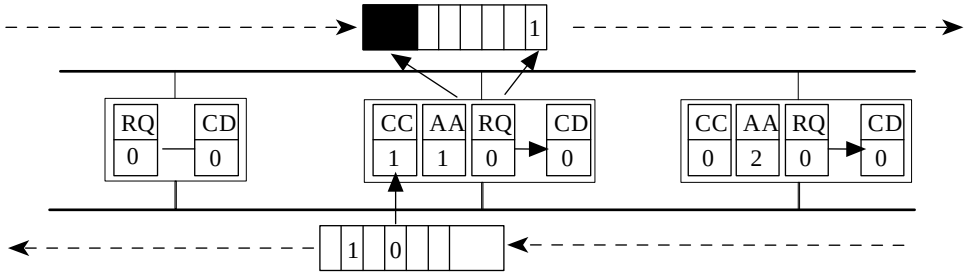


Figure 6: An example of the cell-based flow control.

(6d)



(6e)



(6f)

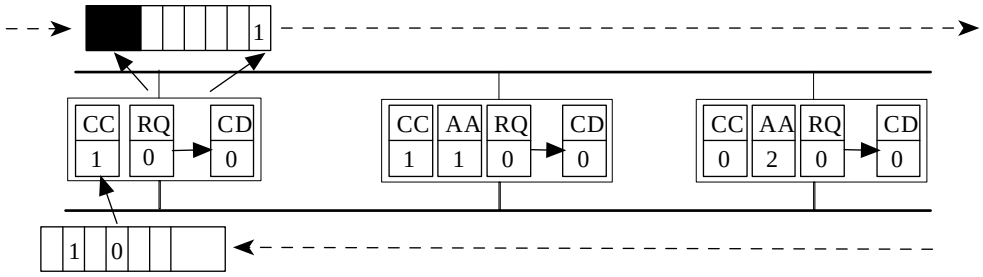


Figure 6: An example of the cell-based flow control (continued).

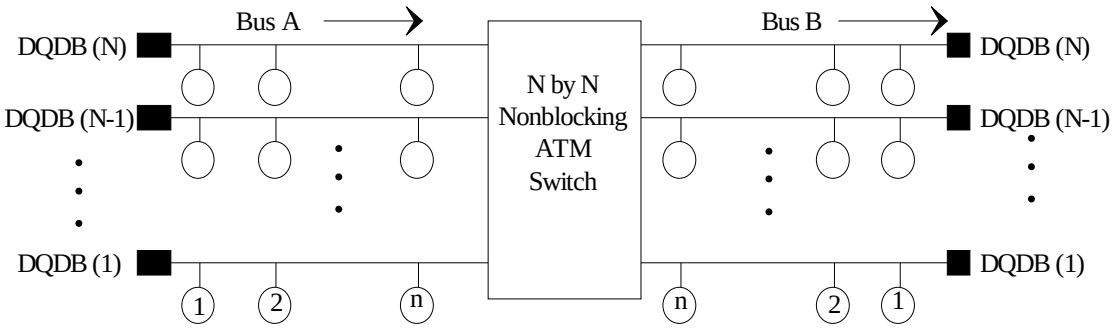


Figure 7: The simulation model of the DQDB interconnection system.

when $ACLR$ equals to zero. With this definition, only a high AST and a low $ACLR$ can produce a high ATM switching efficiency (ASE). When both AST and $ACLR$ are high, the efficiency will be degraded because the cells received by the input buffer are almost retransmitted cells.

4.2 The Simulation Model

The cell-based flow control scheme is implemented by the C programming language on a *Sun SPARC 10* workstation. The simulation model consists of an $N \times N$ ATM switch which interconnects N DQDB subnetworks as shown in Figure 7. The forward (reverse) bus of each DQDB subnetwork is connected to one of the input (output) lines of the ATM switch. The inside of the ATM switch is the same as that in Figure 3. Each input line has an ICF (Input Cell Filter) which is used to absorb local cells from entering the input buffer. Each input buffer has a fixed capacity for holding cells, denoted by b (in unit of cells). Each output line has an OCA (Output Cell Arbitrator) which is used to control the remote/local ratio (denoted by *R/L ratio*). The ATM switching network should be a non-blocking multi-stage interconnection network. We use a *max-min bipartite matching algorithm* [14] to simulate this network. With this algorithm, the maximum number of conflict-free input/output pairs can be obtained and the lengths of all input queues are kept balanced.

For DQDB subnetworks, the message arrival rate of each station is a Poisson distribution and the message length is an exponential distribution. The message length is also in unit of cells. Let $DQDB_i$ represent the i-th DQDB subnetwork connected to the i-th input/output line of the ATM switch, $1 \leq i \leq N$. Let n denote the number of stations in a DQDB subnetwork. Let λ_{ij} represent mean message arrival rate of the j-th station on $DQDB_i$. Then, the *subnetwork message arrival rate* for $DQDB_i$ can be defined by

$$\lambda_i = \sum_{j=1}^{n} \lambda_{ij} \ .$$

The *subnetwork segment arrival rate* for $DQDB_i$ can be defined by

$$\overline{\lambda_i} = \lambda_i \times \ mean\ message\ length \ .$$

Each DQDB subnetwork uses the standard distributed queuing protocol to access the empty slots. The probability of transmitting the remote segment in $DQDB_i$ to $DQDB_j$ ($i \neq j$), is $1/(N-1)$

(uniform distributed excluding the case for $i = j$). The efficiency of the cell-based flow control scheme is observed on the first DQDB subnetwork ($DQDB_1$) according to the following parameters:

1. N = 16;
2. n = 10;
3. Station Distance = 5 slots;
4. The Distance between the ATM switch and the nearest DQDB station = 5 slots;
5. b = 128 to 1;
6. Mean Message Length = 30 segments;
7. R/L ratio = 8/1, 5/1, 2/1, 1/1, and 1/2;
8. LOSS_PENALTY = 100;

4.3 The Optimal Input Buffer Size

In this section, the minimum input buffer size for gaining an optimal cell processing throughput is investigated. To optimally design a flow control under heavy load, the cell arrival rate in the ATM input buffer should be matched with the cell departure rate (cell processing rate), and in the mean time, the input buffer size is minimized. Assume that there is only one station in the DQDB subnetwork and the round-trip delay from the station to the ATM input buffer is d (in unit of cells). In order to balance the cell arrival rate and the cell departure rate in the ATM input buffer, the credit generating rate in the ATM switch should be equal to or greater than the cell departure rate. Assume that the cell departure rate is ρ (per slot time) and the input buffer size is b (in unit of cells), then at most b credits can be sent within every d slot time. Thus, the credit generating rate is at most

$$b/d\ .$$

Since we require $b/d \geq \rho$, we have

$$b \geq d\rho\ .$$

In the DQDB interconnection system, the average cell departure rate is $R/(R + L)$ (since the traffic is uniformly distributed). Therefore, the optimal input buffer size is

$$\frac{dR}{R+L}\ .$$

5 Simulation Results

The performance of the interconnection system without any flow control is observed first. In Figure 8, the average switching efficiency of the ATM switch with respect to different $\overline{\lambda_1}$ is presented, where b is set to 100. The result is an average of 20000 slot times after an initial execution of 20000 slot times.

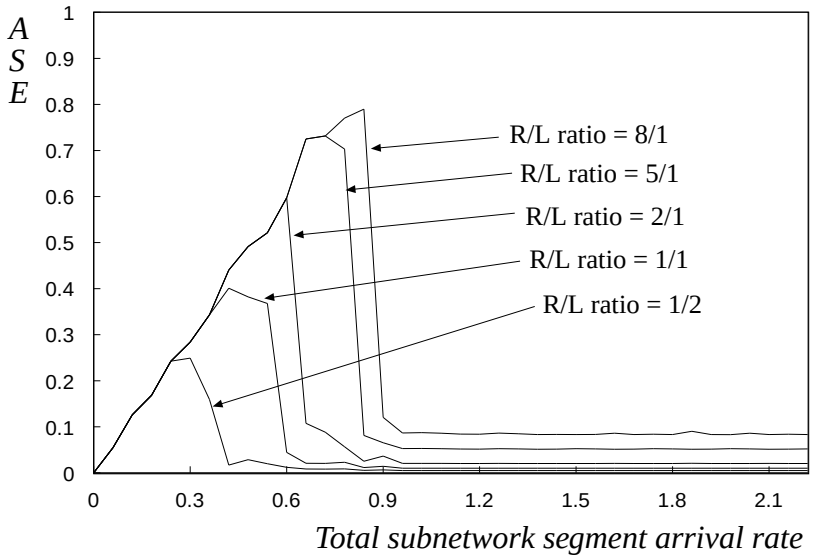


Figure 8: The average switching efficiency of the ATM switch for different $\overline{\lambda_1}$ under no flow control.

The performance is very poor when the total subnetwork arrival rate is greater than $R/(R+L)$. This is because that the cell loss rate in the ATM switch is quite high.

The performance of the interconnection system after applying the cell-based flow control scheme is shown in Figure 9 throughout Figure 14. In Figure 9, the average switching efficiency of the ATM switch with respect to different $\overline{\lambda_1}$ is presented, where b is set to 100. The performance is improved significantly. This result shows that the *ASE* always matches with the *AST* under different total subnetwork arrival rates since the *ACLR* is always zero. Furthermore, the *ASE* under heavy load always matches with the ATM cell processing rate $R/(R+L)$. This means that the cell-based flow control scheme can reach the optimal switching throughput such that no cell is lost.

In Figure 10, the average switching efficiency of the ATM switch with respect to different b is presented, where $\overline{\lambda_1}$ is set to 1.0. The result shows that the throughput converges to $R/(R+L)$ when b is equal to or greater than $R/(R+L) \times 50$. This matches with the result in section 4 since 50 is the average round-trip delay between the ATM switch and the DQDB stations.

In Figure 11, the average switching efficiency of the ATM switch with respect to different $\overline{\lambda_1}$ is presented, where R/L is set to $8/1$ and b is set to $1, 5, 10, 20, 30, 40, 50, 70$ and 90. When b is smaller than 50, the *ASE* is approximately equal to $\frac{R}{R+L} \times \frac{b}{50}$. This means that the proposed flow control scheme can result in optimal throughput when the size of the input buffer is limited. A close-up of Figure 11 is presented in Figure 12.

In Figure 13, the average switching efficiency of the first input buffer is presented when the ATM cell processing rate is dynamically changed. Assume that $\overline{\lambda_1} = 1.0$. At time = 0, the R/L ratio is set to $8/1$. At time = 5000th slot, the R/L ratio is changed into $1/1$ and at time = 10000th slot, the R/L ratio is changed into $2/1$. The result shows that the cell-based flow control scheme can always keep the cell arrival rate matched with the cell processing rate dynamically.

The throughput of the DQDB subnetwork is also observed. The *TDT* of $DQDB_1$ and the *DST* of each station are shown in Figure 14 when the stations are activated or deactivated at different time. The

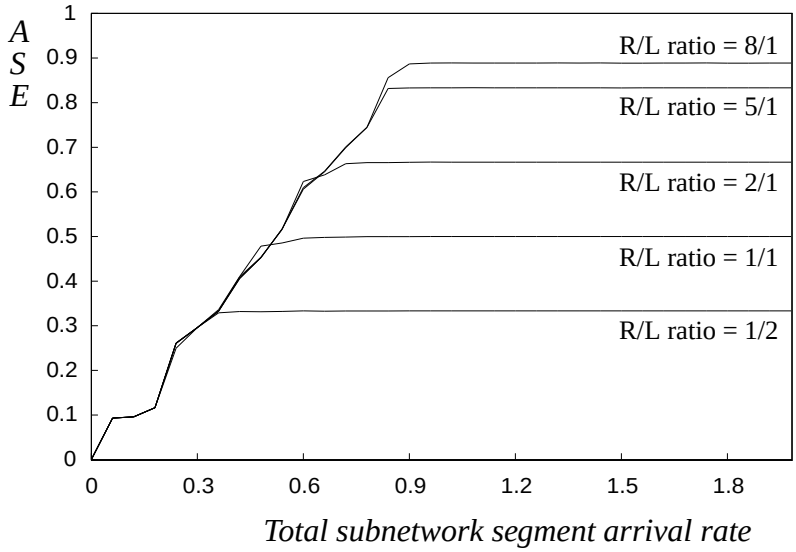


Figure 9: The average switching efficiency of the ATM switch for different $\overline{\lambda_1}$ under cell-based flow control.

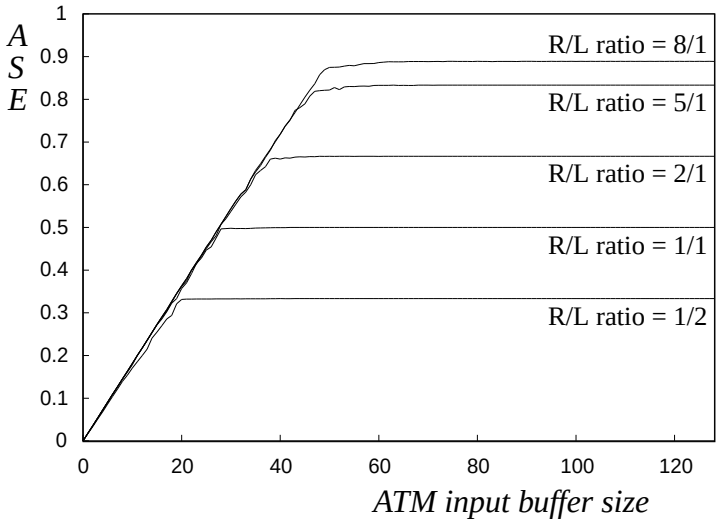


Figure 10: The average switching efficiency of the ATM switch for different b under cell-based flow control.

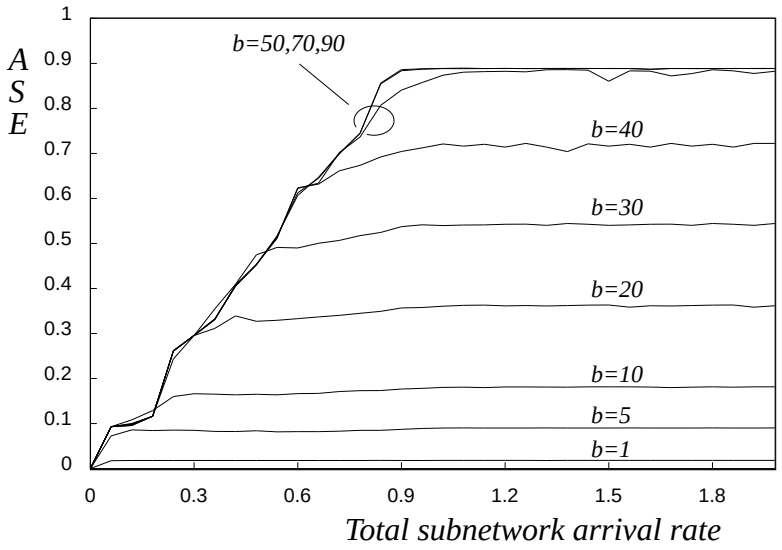


Figure 11: The average switching efficiency of the ATM switch for different $\overline{\lambda_1}$ under cell-based flow control.

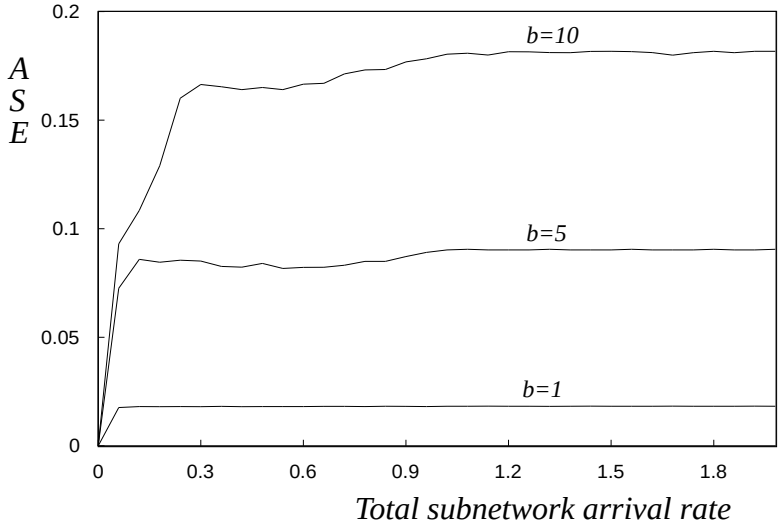


Figure 12: The close-up of Figure 11.

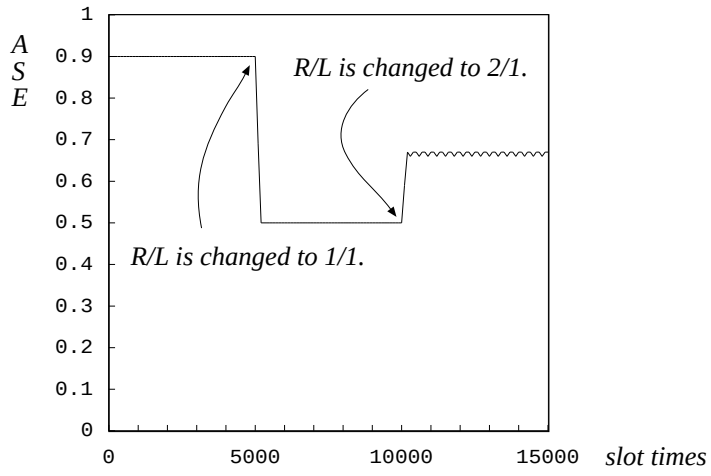


Figure 13: The average switching efficiency of the ATM switch for dynamic ATM cell processing rate.

activating or deactivating time are listed as follows.

1. At time = 0, station 5 becomes active.
2. At time = 6000th slot, station 10 becomes active.
3. At time = 10000th slot, station 3 becomes active.
4. At time = 14000th slot, station 5 becomes inactive.
5. At time = 17000th slot, stations 1 and 6 become active.

In this case, the R/L ratio is set to $8/1$ and the message arrival rate of each station in active state is 0.05 (heavy loaded). All other DQDB subnetworks are also heavy loaded and assume that only remote segments are transmitted. The result shows that the bandwidth is fairly shared dynamically by each active station on the DQDB subnetwork. In the mean time, the total subnetwork throughput is about 0.9, which is approximately equal to $\frac{R}{R+L} = \frac{8}{9}$.

6 Conclusions

In this paper, a distributed dual bus approach is proposed for interworking between multiple IWUs of the legacy LANs and the ATM networks. Heterogeneous LANs can also interwork with each other via the dual bus topology as well as the interworking with the ATM. The essential part of the proposed method is a flow control scheme called cell-based flow control which is a novel approach instead of traditional window-based or the rate-based schemes. The resulting system is strongly reliable since no cell is lost. Furthermore, the switching efficiency of the ATM switch is maximized under limited input buffer. The simulation results also show that the bandwidth of the DQDB subnetwork can be fairly and dynamically shared by the active stations.

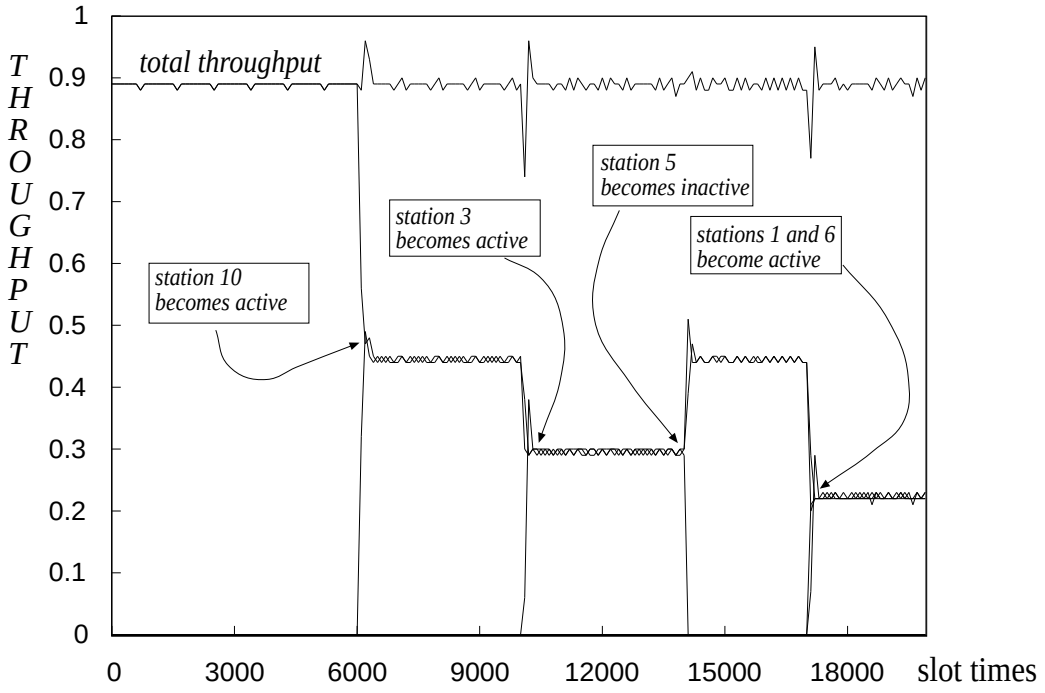


Figure 14: The bandwidth allocation of a flow-controlled DQDB subnetwork.

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